DESIGN OF A PIPELINED MULTIPLIER CHIP AS THE KERNEL OF A VECTOR PROCESSING ARCHITECTURE

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ABSTRACT

This paper describes the design of a pipelined multiplier chip, named TREVO. This chip constitutes a major element in a vector processing architecture, which is being researched in the Instituto de Informática of the Federal University of Rio Grande do Sul - Brazil, in the context of the Cp2 project.

KEY WORDS

pipeline - vector architecture - VLSI chip design - multiplier - Cp2

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I. INTRODUCTION

The huge increase of computer performance nowadays is due to new architectural concepts and to microelectronics technology developments.

In the Instituto de Informática of the Federal University of Rio Grande do Sul (II/UFRGS) is being developed the Cp2 project (Parallel Processing Contributions) which is intented to strongly contribute to the parallel processing area.

One of the major research topics of Cp2 is the development of a vector processing architecture.

The strategy in the design of such computer is to merge advanced research concepts belonging to the Microelectronics and the Computer Architecture fields.

This paper is divided in two main parts:

- the first one describes TREVO: a pipelined 4x4 bits multiplier;
- the second one describes how the TREVO chip is employed in a vector processing architecture:

II. TREVO DESIGN

One of the most important projects under development by the Microelectronics Group (GME) of the II/UFRGS is named CIPREDI (PRE-DIFfUSED INTEGRATED CIRCUITS), which deals with innovative methodologies to the design of gate array circuits, especially sea of gates. CIPREDI's main axis of research concentrate both on VLSI chip design and on CAD tools.

After the design of the complex PEALO circuit (directed memory controller for INTEL 8085 microprocessor), the CIPREDI team judged important to design chips which employ parallel mechanisms.

In this sense, the design of the TREVO chip was launched. This circuit is aimed to perform parallel multiplications, using the pipeline technique. As a first step in this domain and due to silicon area limitations in multiple project-chips runs, a decision was taken to consider only 4x4 bits multiplications: TREVO consists then of a 4x4 bits pipeline combinatorial multiplier chip.

The multiplication algorithm employed by TREVO is showed in figure 1.

				a_3	a_2	a_1	a_0	=A
				b_3	b_2	b_1	b_0	=B
				a_3b_0	a_2b_0	a_1b_0	a_0b_0	=W_1
			a_3b_1	a_2b_1	a_1b_1	a_0b_1		=W_2
		a_3b_2	a_2b_2	a_1b_2	a_0b_2			=W_3
	a_3b_3	a_2b_3	a_1b_3	a_0b_3				=W_4
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0	=AxB=P

Fig. 1:TREVO's multiplication algorithm

To produce this multiplication the designers divided the circuit into four stages:

- the first one formed only by and gates, producing intermediate results;
- the second one, formed only by carry save adder (CSA) blocks [1], producing intermediate results;
- the third one, formed only by CSA blocks, producing intermediate results; and

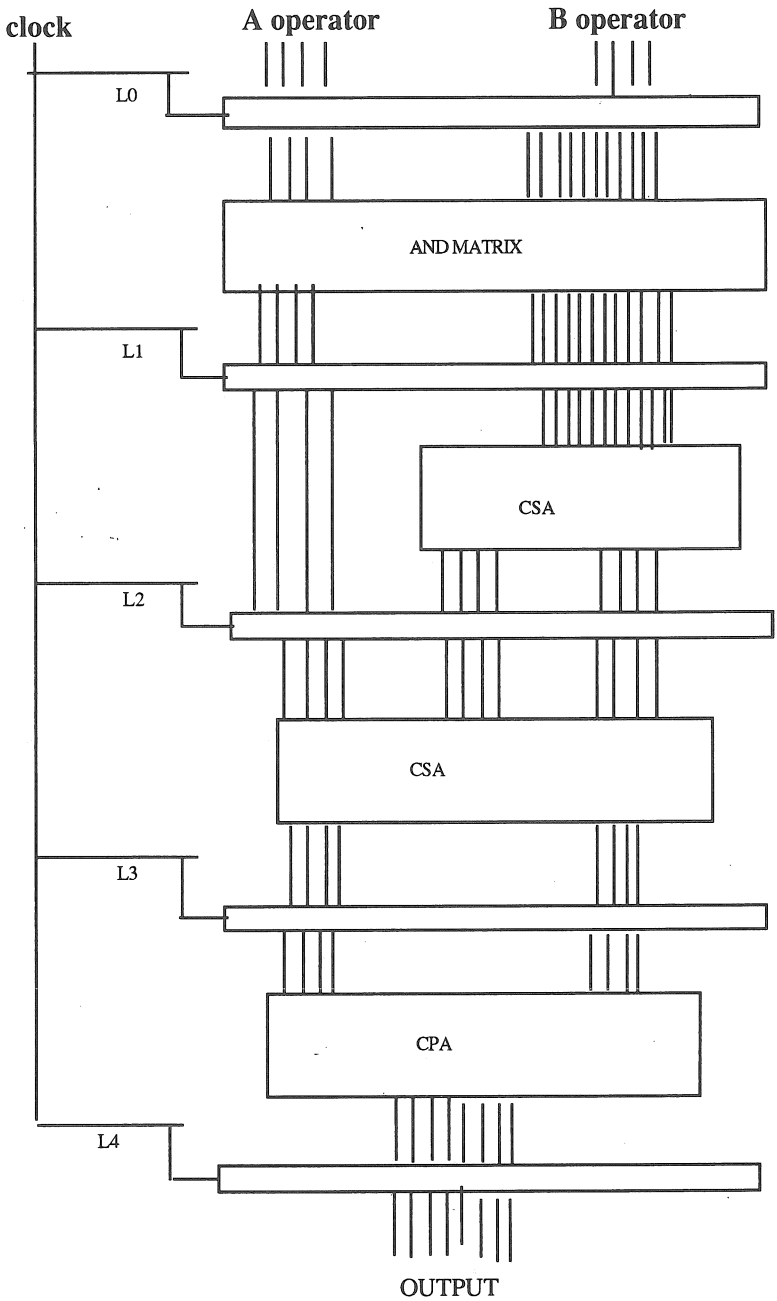

Fig. 2 - TREVO's logic architecture

- the fourth one, formed by carry-propagate adder (CPA) blocks, producing the final results.

The pipeline operation becomes natural, providing parallel execution by the four present stages. The logic diagram of TREVO's architecture is showed in figure 2.

The cells employed by TREVO belong to the CMOS 2,0 mm CIPREDI's library [2]. Basically the chosen cells are: AND, HALF-ADDER, FULL-ADDER and EDGE-SENSITIVE LATCH.

The maximum clock signal frequency imposable to the circuit derives directly from the slowest stage. In this case, as the CPA block (4th stage) presents the highest expected delay (50 ns), this imposes a maximum 20 MHz clock rate.

In each clock pulse each stage's latch capture data from the previous stage. In this sense, the circuit can perform until 20 millions multiplications per second (MOPS),in the case of correct data buffering.

The expected performance of this chip suggests its utilisation in vector operations taking advantage of its high multiplication speed.

III. VECTOR PROCESSING ARCHITECTURE

In the vector processing architecture design the first guideline addressed consistad how to deal withthe 20 MIPS rate, providing to the TREVO chip, 20 MWords/s as input and 20 MWords/s as output, providing then a total 40 MWords/s data rate. The time between words becomes 25 ns, which cannot be supported by a simple main memory, forcing the interleaved acces memory strategy. This leads to buffer the input data or output data allowing the main memory to deal only with read operations or with write operations during fixed slots of time.

Considering that the multiplier pumps 20 MW/s and drives other 20 MW/s, it becomes interesting to design the register system to accomodate vectors.

In this sense the pipeline (the TREVO chip initially) could operate simultaneously with register files: two to receive input data other one to receive the output processed data and another one can be used to receive a new data vector. When the multiplication finishes the pipeline begins to multiply data from an register buffer described above.

This configuration could allow steady maximum speed in the multiplication of large data vectors, even if they are much bugger than the register file length. This implies a minimum of four vector register files. In the computer under development, this number was used.

It must be noted that at each filling or empting of a vector register file the interleaved memory must change from the read to the write condition. This interrupts the data sequence forcing a reinitialization of the memory access. This imposes a speedup diminution equal to the number of memory modules.

For instance if the interleaved memory system disposes of eight modules exchanging data with a N-element register file the final system performance will be of N/N+8, in respect of the ideal performance. Using this relationship different main memory system utilisation efficiences were calculated for different vector regrater leythe (as chawn in table 1).

Vector Register Length (Number of 8 bit registers)	Memory utilization relative efficiency
16	66,6%
32	80%
64	88.8%
128	94.1%
256	96.9%
512	98.4%

Table 1: Memory utilization relative efficiency x Vector Register Length

From this table, it can be visualized that solutions which employ vector registers with lengths higher or equal to 128 elements allow great main memory profit.

In the design it was taken the 256 register lenght and the parameter explaired above of 4 vector register files. This produces a 1K (256 x 4) positions buffer memory.

In this paper the off the shelf circuits employed in the organization of the proposed architecture are not presented, but can be found in [3].

IV. CONCLUSIONS

At a first glance, it can be considered that the designed architecture presents only restricted applicability since it performs only one kind of operation.

Nevertheless, if other operative and logical parts are added to this architecture as pipelined adder/subtractor and a superscalar ULA (towards a VLIW processor), this project could perform many useful vector operations.

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